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Design and Implementation of Multibit Flip flops by Using Single Phase Adiabatic Clock

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ABSTRACT
As technology advances, a system on chip (SOC) design can contain more and more components that lead to a high power density. Now-a-days in IC's, the power consumed by clocking gradually takes a dominant part. . Power, Area, Performance has become a main issue in VLSI design. In previous designs they have performed a co-ordinate transformation to identify the flip-flops that can be merged and their legal regions. A combinational table is formed by that flip-flops. Finally they used hierarchical way to merge the flip-flops. Due to this design the power consumption can be reduced by replacing some flip-flops by fewer multi-bit flip-flops. We have proposed an single phase adiabatic clock in for further reduction of the power. In our design also first we will identify the mergeable flip-flops, build a combinational table from mergeable flip-flops and all the flip-flops are divided into sub regions to check whether they are working properly or not and finally these flip-flops are combined together, at this point we are giving an single phase adiabatic clock as input to those flip-flops for the reduction of power consumption and timing.

Index Terms **--** Clock power reduction, merging, multi bit flip-flops, Adiabatic clock

I. Introduction

As technology advances, an system on chip (SOC) design can contain more and more components that leads to high power density [1]. A heavy growth recently has done by portable multimedia and communication devices. Main advantage of these products is long battery life. In many products, main portion of circuits is occupied by multi-bit flip flops and delay buffers. By reducing the power consumption, we can increase battery life and also we can reduce the overheating problem of the circuit, but increases packaging or cooling. Therefore, the consideration of power consumption in complex SOCs has become a heavy challenge to designers. Now-a-days VLSI designs, power consumed by clocking has taken a maximum portion of the whole design especially for those who design deeply scaled CMOS technologies.

Thus, several methodologies have been proposed to reduce the power consumption of clocking. In the recent years, as the process technology advances, feature size of IC is shrank, the minimum size of clock drivers can trigger more than one flip-flop [3].

The required circuit and the power consumption can be reduced, when smaller flip-flops are replaced by larger bits of multi flip-flops[2].

In previous designs they have performed a co-ordinate transformation to identify the flip-flops which can be merged. A combinational table is formed by that flip-flops. Finally hierarchical way is used to merge the flip-flops. By using this design the power consumption is reduced by replacing some flip-flops by fewer multi-bit flip-flops. In our proposed design a single phase adiabatic clock is used for further reduction of the power and timing.

1.1 Multi-Bit Flip-Flops

Combination of two or more flip flops is known as multi-bit flip flops. In multi-bit flip flops a single clock is shared between all flip flops, due to this power consumption can be reduced.

A single-bit flip-flop has two latches (Master latch and slave latch). The latches need "Clk" and "Clk' " signal to perform operations.

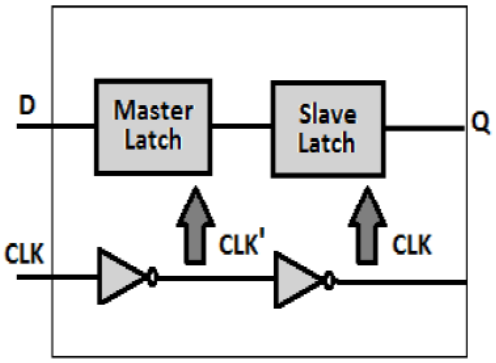


Fig 1.1(A) Single bit flip-flop

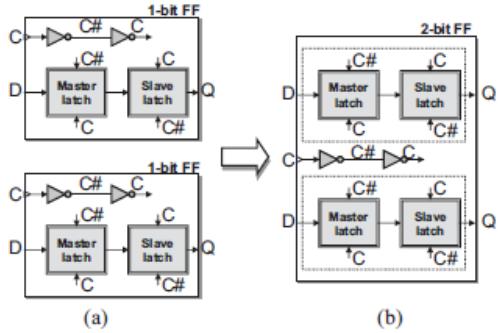


Fig 1.1(B) Example of merging two 1-bit flip-flops into one 2-bit flip-flop.
(a) Two 1-bit flip-flops (before merging). (b) 2-bit flip-flop (after merging).

Multi-bit flip-flop cells are capable of decreasing the power consumption because they have shared Inverter inside the flip-flop and they can minimize clock skew at the same time. To obtain these benefits, the ASIC design must meet the following requirements. The single-bit flip-flops we want to replace with multi-bit flip-flop must have same clock condition and same set/reset condition.

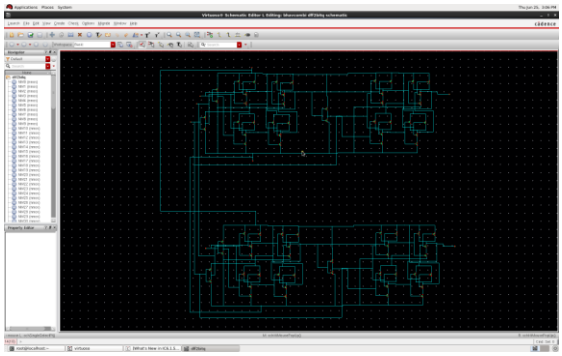


Fig 1.1(C) Schematic of 2bit flip-flop

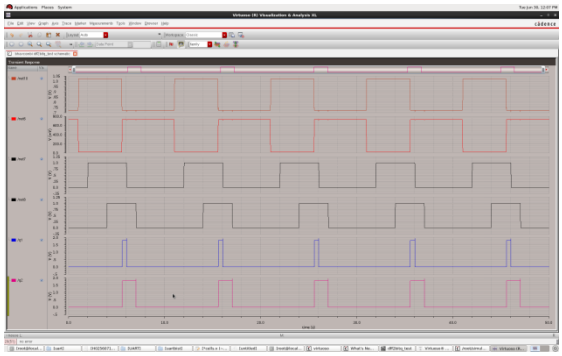


Fig 1.1(D) Waveform of 2bit flip-flop

II. Adiabatic Logic

In modern computer system design power, area and timing consumption became a high. During past years several effective power management design techniques have been developed.

The word adiabatic is taken from Greek language which means "impassible" and implies the thermodynamic principle of state change with no loss of gain or heat [5].

2.1 Purpose of Adiabatic logic

Adiabatic switching is also known as alternative CMOS logic, with no loss or gain of energy.

The below circuits operates when given supply is given at vdd.When the input supply is given at in then the output is appeared at outbar. The output will be hign when the input supply is given at inbar . This circuit operates when the vdd voltage is not greater that 1.8v [6].

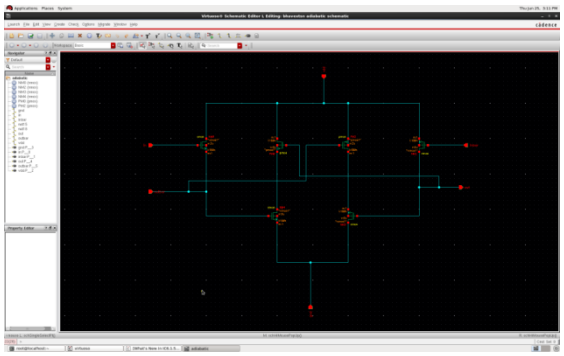


Fig 2.1(a) Schematic of Adiabatic circuit

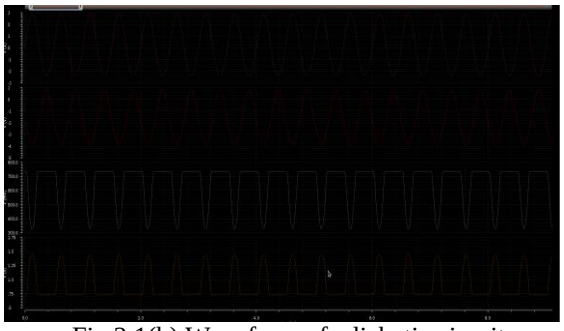


Fig 2.1(b) Waveform of adiabatic circuit

III. Formulation of problem

3.1 Identification of Mergeable Flip-flops

The identification of mergeable flip flops can be done by using binary tree concept.

In computer science, a binary tree is defined as tree data structure. In binary tree format each node has at most two children, they are left child and the right child. From a graph theory, binary (and K-ary) trees as defined as arborescences. A binary tree is also known as bifurcating arborescence a term which actually appears in some very old programming books, before the modern computer science terminology. It is also possible to interpret a binary tree as an undirected, rather than a directed graph, in which case a binary tree is an ordered, rooted tree. A binary tree is a special case of an ordered K-ary tree, where k is 2.

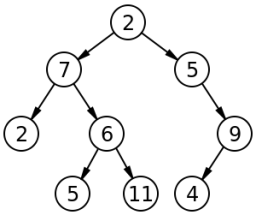
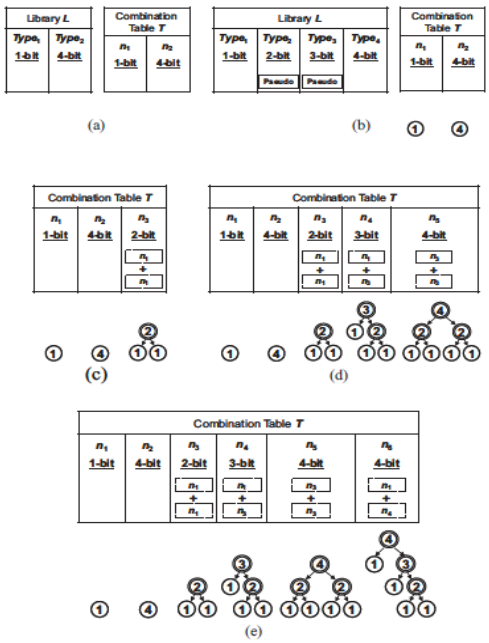


Fig 3.1 Example of labelled binary tree

3.2 Combinational Table

We will build a combination table, which records all possible combinations of flip-flops to get feasible flip-flops before replacements. Thus, we can replace flip-flops depending on the combinational table. Each time we use only one combination of flip-flops, to reduce the search time [1].

For simplicity we use a binary tree to represent one combination.. A flip-flop in ***L*** is demoted by each node in the tree. The types of flip-flops denoted by leaves will constitute the type of the flip-flop in the root. For each node, the bit width of the corresponding flip-flop equals to the bit width summation of flip-flops denoted by its left and right child. In the beginning, we initialize a combination ni for each kind of flip-flops in L (. Then, in order to represent all combinations by using a binary tree, we may add pseudo types, which denote those flip-flops that are not provided by the library. For example, assume that a library only supports two kinds of flip-flops whose bit widths are 1 and 4, respectively. In order to use a binary tree to denote a combination whose bit width is 4, there must exist flip-flops whose bit widths are 2 and 3 in L.Thus, we have to create two pseudo types of flip-flops with 2- and 3-bit if L does not provide these flip-flops.



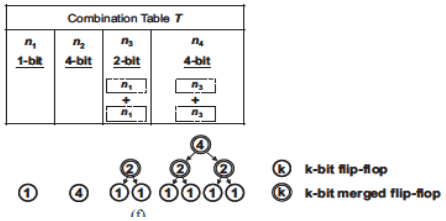


Fig 3.2(A). Example of building the combination table. (a) Initialize the library *L* and the combination table *T* . (b) Pseudo types are added into *L*, and the corresponding binary tree is also build for each combination in *T*. (c) New combination *n*3 is obtained from combining two *n*1s. (d) New combination *n*4 is obtained from combining *n*1 and *n*3, and the combination *n*5 is obtained from combining two *n*3s. (e) New combination *n*6 is obtained from combining *n*1 and *n*4. (f) Last combination table is obtained after deleting the unused combination in (e).

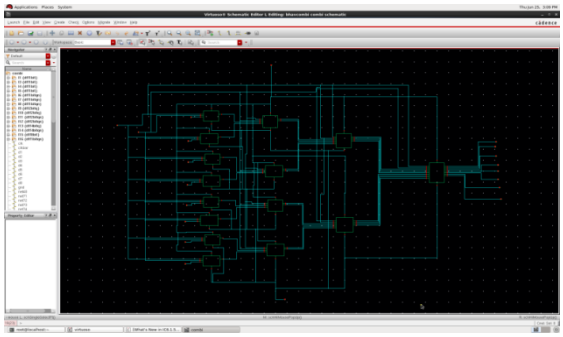


Fig 3.2(B) Schematic of 8bits using combinational table

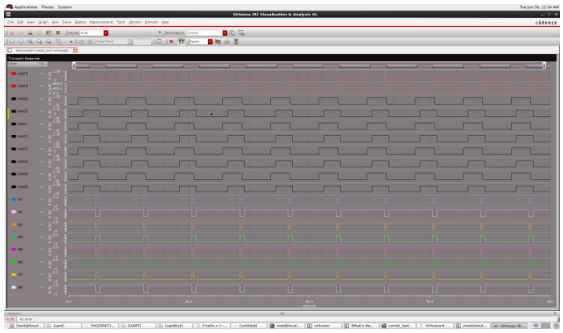


Fig 3.3(C) waveform of 8bits using combinational table

3.4 Merging of flip-flops

To reduce the complexity, we first divide the whole placement region into several sub regions, and use the combination table to replace flip-flops in each sub region. Then, several sub regions are combined into a larger sub region and the flip-flops are replaced again so that those flip-flops in the neighbouring sub regions can be replaced further. Finally, those flip-flops with pseudo types are deleted in the last stage because they are not provided by the supported library [1].

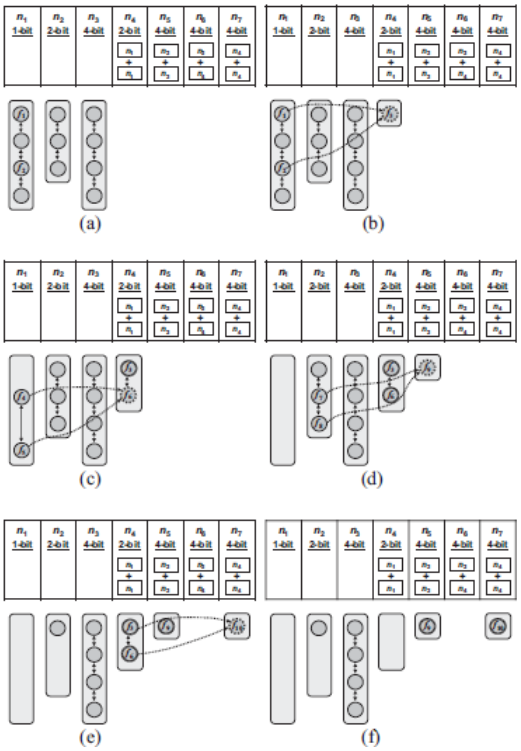


Fig 3.4(A). Example of replacements of flip-flops. (a) Sets of flip-flops before merging. (b) Two 1-bit flip-flops, *f*1 and *f*2, are replaced by the 2-bit flip-flop *f*3. (c) Two 1-bit flip-flops, *f*4 and *f*5, are replaced by the 2-bit flip-flop *f*6. (d) Two 2-bit flip-flops, *f*7 and *f*8, are replaced by the 4-bit flip-flop *f*9. (e) Two 2-bit flip-flops, *f*3 and *f*6, are replaced by the 4-bit flip-flop *f*10. (f) Sets of flip-flops after merging.

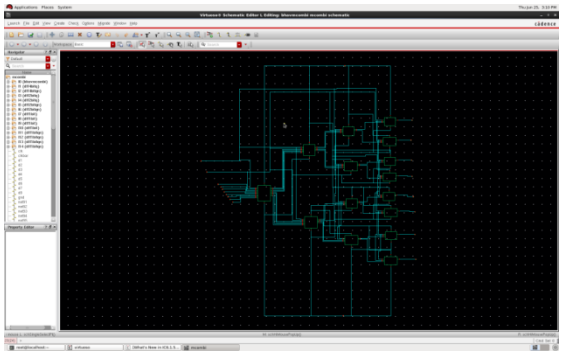


Fig 3.4(B) Merging of 8bit flip-flops

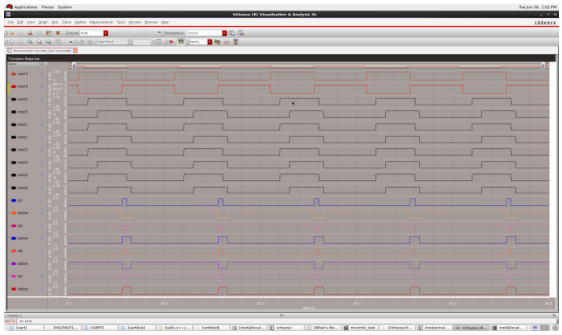


Fig 3.4(C) Waveform of 8bits of merging flip-flops

3.5 Addition of adiabatic clock to merging flip-flops

Adiabatic clock is used for power reduction in sequential circuits. Adiabatic clock resembles a sine wave.

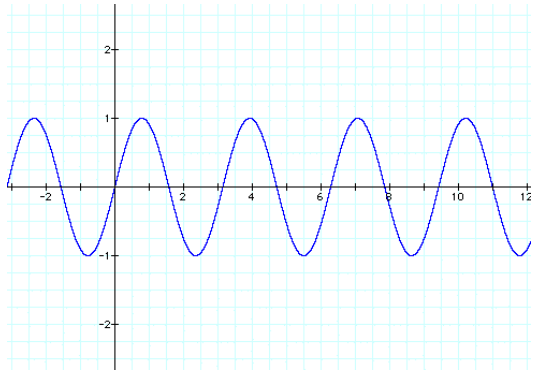


Fig 3.5(A) Sine wave which resembles an adiabatic clock

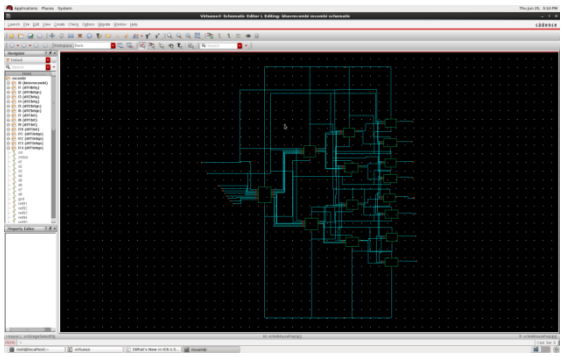


Fig 3.5(B)Addition of adiabatic clock to merging flip-flops

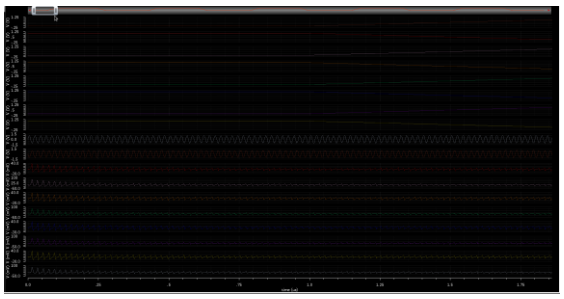


Fig 3.5(C) Waveform of adiabatic clock

IV. Results

Power calculations and timing is shown in below table

Power and Timing	Combination of 8bit flip flops	Merging of 8bit flip flops	Using Adiabatic clock
Power(W)	2.515E-3	770.6E-6	697.6E-6
Timing(s)	0.15	0.15	0.02

Table 4. Power and Timing calculations for different regions

V. Conclusion

Identification of mergeable flip flops can be done by using binary tree format and later those megeable flip flops are formed as multi-bits by using combinational table until further reduction of flip flops cannot be done. By using combinational table the flip flops are merged to check whether those flip flops are working properly or not. From the above results we can conclude that power and timing are reduced by using single phase adiabatic clock. As the multi-bits increases the power consumption and timing also reduces using adiabatic clock.

References

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